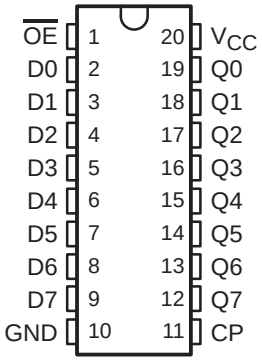
CD74HCT574-EP
HIGH-SPEED CMOS LOGIC OCTAL D-TYPE FLIP-FLOP 3-STATE, POSITIVE-EDGE TRIGGERED

SCLS571 − FEBRUARY 2004

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of −40°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree†**
- **Buffered Inputs**
- **Common 3-State Output-Enable Control**
- **3-State Outputs**
- **Bus-Line Driving Capability**
- **Typical Propagation Delay (Clock to Q): 15 ns at V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . 15 LSTTL Loads**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **V_{CC} Voltage = 4.5 V to 5.5 V**
- **Direct LSTTL Input Logic Compatibility, V_{IL} = 0.8 V (Max), V_{IH} = 2 V (Min)**
- **CMOS Input Compatibility, $I_I \leq 1\ \mu A$ at V_{OL}, V_{OH}**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

M OR PW PACKAGE
(TOP VIEW)



description/ordering information

The CD74HCT574 is an octal D-type flip-flop with 3-state outputs and the capability to drive 15 LSTTL loads. The eight edge-triggered flip-flops enter data into their registers on the low-to-high transition of the clock (CP). The output enable ($\overline{OE}$) controls the 3-state outputs and is independent of the register operation. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

ORDERING INFORMATION

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 125°C	SOIC − M	Tape and reel	CD74HCT574QM96EP	HCT574EP
	TSSOP − PW	Tape and reel	CD74HCT574QPWREP	HCT574EP

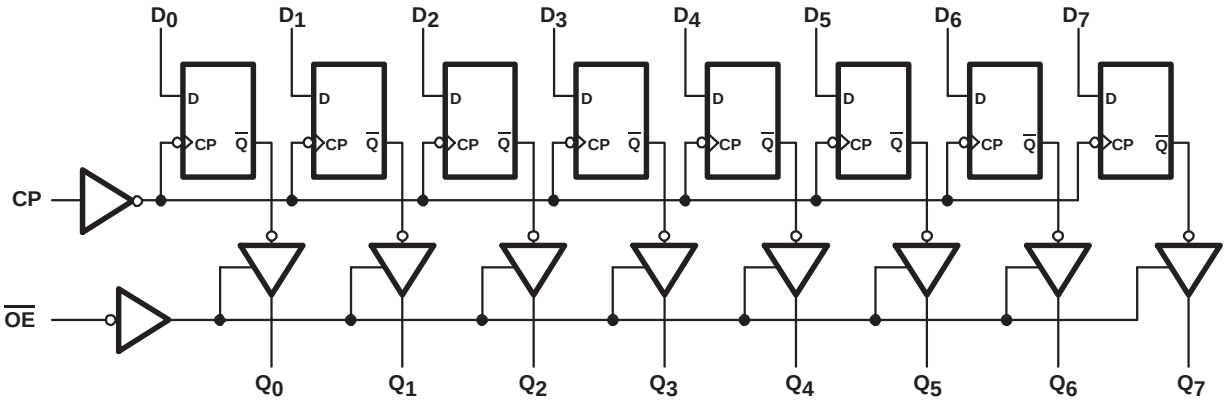
‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	CP	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

NOTE: H = High voltage level (steady state)
L = Low voltage level (steady state)
X = Don't care
↑ = Transition from low to high level
Q_0 = Level before the indicated steady-state conditions were established
Z = High-impedance state

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) . . . . . ±20 mA
Drain current per output, I_O ($V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) . . . . . ±35 mA
Output source or sink current per output, I_O ($V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) . . . . . ±25 mA
Continuous current through V_{CC} or GND, I_{CC} . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): M package . . . . . 58°C/W
PW package . . . . . 69°C/W
Maximum junction temperature, T_J . . . . . 150°C
Lead temperature (during soldering):
At distance 1/16 ± 1/32 inch (1,59 ± 0,79 mm) from case for 10 s max . . . . . 300°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages referenced to GND unless otherwise specified.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0	1000	ns
		V_{CC} = 4.5 V	0	500	
		V_{CC} = 6 V	0	400	
T_A	Operating free-air temperature		−40	125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		I_O (mA)	V_{CC}	T_A = 25°C			T_A = −40°C TO 125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	CMOS loads	−0.02	4.5 V	4.4			4.4		V
		TTL loads	−6	4.5 V	3.98			3.7		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	CMOS loads	0.02	4.5 V			0.1		0.1	V
		TTL loads	6	4.5 V			0.26		0.4	
I_I	$V_I = V_{CC}$ or GND		0	5.5 V			±0.1		±1	µA
I_{OZ}	$V_I = V_{IL}$ or V_{IH},	$V_O = V_{CC}$ or GND		6 V			±0.5		±10	µA
I_{CC}	$V_I = V_{CC}$ or GND		0	5.5 V			8		160	µA
ΔI_{CC}	$V_I = V_{CC}$ − 2.1 V,	See Note 4		4.5 V to 5.5 V		100	360		490	µA
C_{IN}	C_L = 50 pF						10		10	pF
C_{OUT}	3-state						20		20	pF

NOTE 4: For dual-supply systems, theoretical worst-case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT input loading

TYPE	INPUT	UNIT LOADS†
'574	D0−D7	0.4
	CP	0.75
	$\overline{OE}$	0.6

† Unit load is ΔI_{CC} limit specified in electrical characteristics table, e.g., 360 µA max at 25°C.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER		V_{CC}	T_A = 25°C		T_A = −40°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	4.5 V	30		20		MHz
t_w	Clock pulse duration	4.5 V	16		24		ns
t_{su}	Setup time, data before clock↑	4.5 V	12		18		ns
t_h	Hold time, data after clock↑	4.5 V	5		5		ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

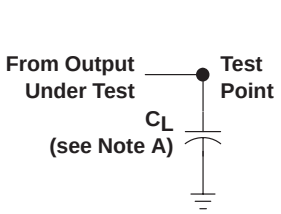
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C			T_A = −40°C TO 125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
t_{pd}	CP	Q	C_L = 50 pF	4.5 V			33		50	ns
			C_L = 15 pF	5 V		15				
t_{dis}	$\overline{OE}$	Q	C_L = 50 pF	4.5 V			28		42	ns
			C_L = 15 pF	5 V		11				
t_{en}	$\overline{OE}$	Q	C_L = 50 pF	4.5 V			30		45	ns
			C_L = 15 pF	5 V		12				
t_t		Q	C_L = 50 pF	4.5 V			12		18	ns
f_{max}	CP		C_L = 15 pF	5 V		60				MHz

operating characteristics, V_{CC} = 5 V, T_A = 25°C, input t_r, t_f = 6 ns

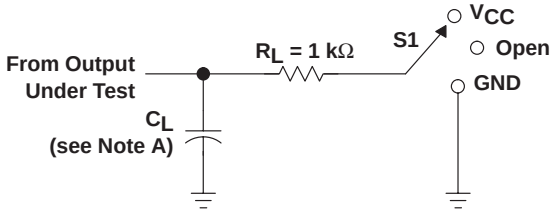
PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance (see Note 5)	47	pF

NOTE 5: C_{pd} is used to determine the dynamic power consumption (P_D), per package.
$P_D = (C_{PD} \times V_{CC}^2 \times f_I) + \Sigma (C_L \times V_{CC}^2 \times f_O)$
f_I = input frequency
f_O = output frequency
C_L = output load capacitance
V_{CC} = supply voltage

PARAMETER MEASUREMENT INFORMATION

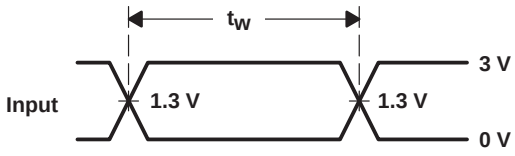


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

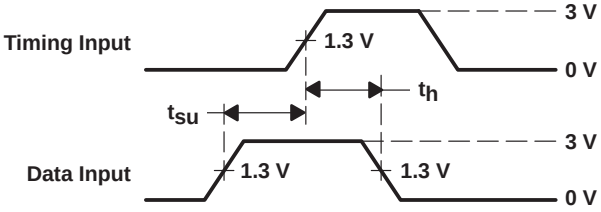


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

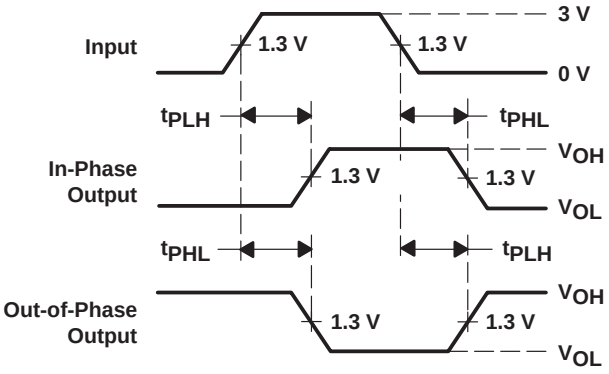
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



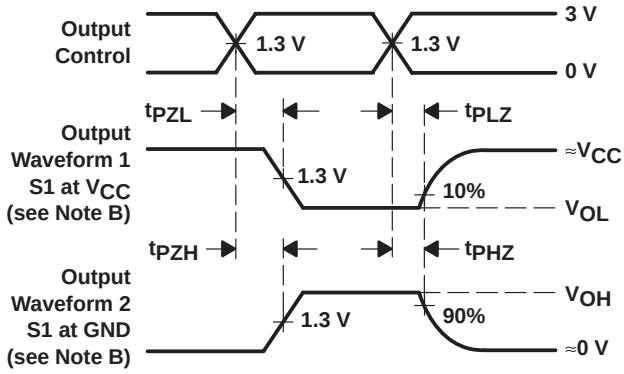
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.
F. t_{PLH} and t_{PHL} are the same as t_{pd}.
G. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
H. t_{PZH} and t_{PZL} are the same as t_{en}.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CD74HCT574QM96EP	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT574QPWREP	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04739-01XE	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04739-01YE	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

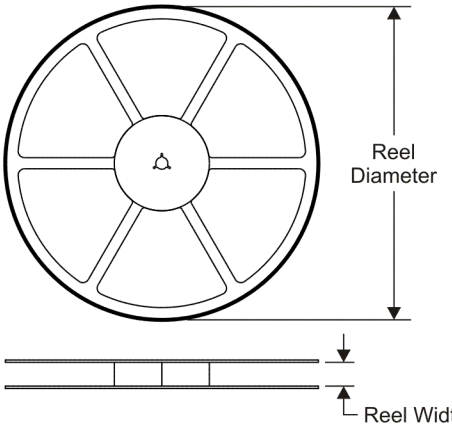
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF CD74HCT574-EP :
- Catalog: CD74HCT574
- Automotive: CD74HCT574-Q1
- Military: CD54HCT574

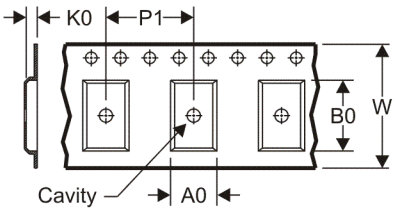
NOTE: Qualified Version Definitions:
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

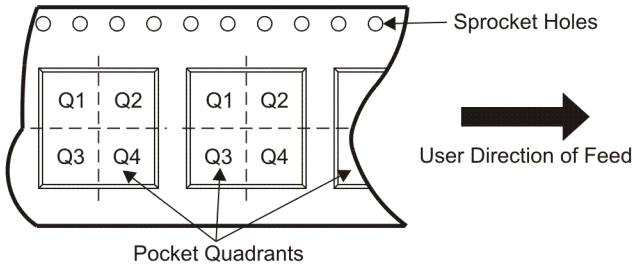


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

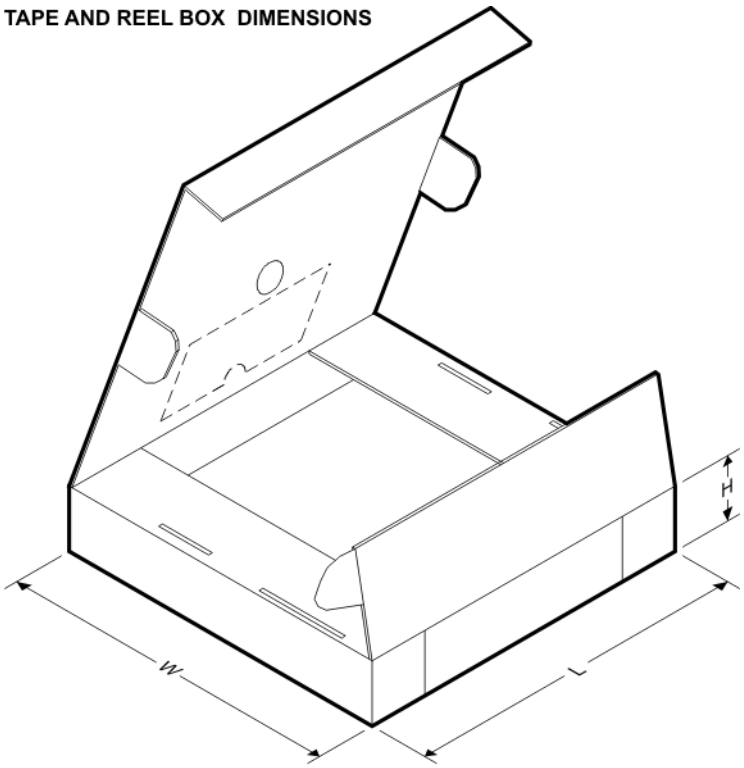
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HCT574QM96EP	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CD74HCT574QPWREP	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

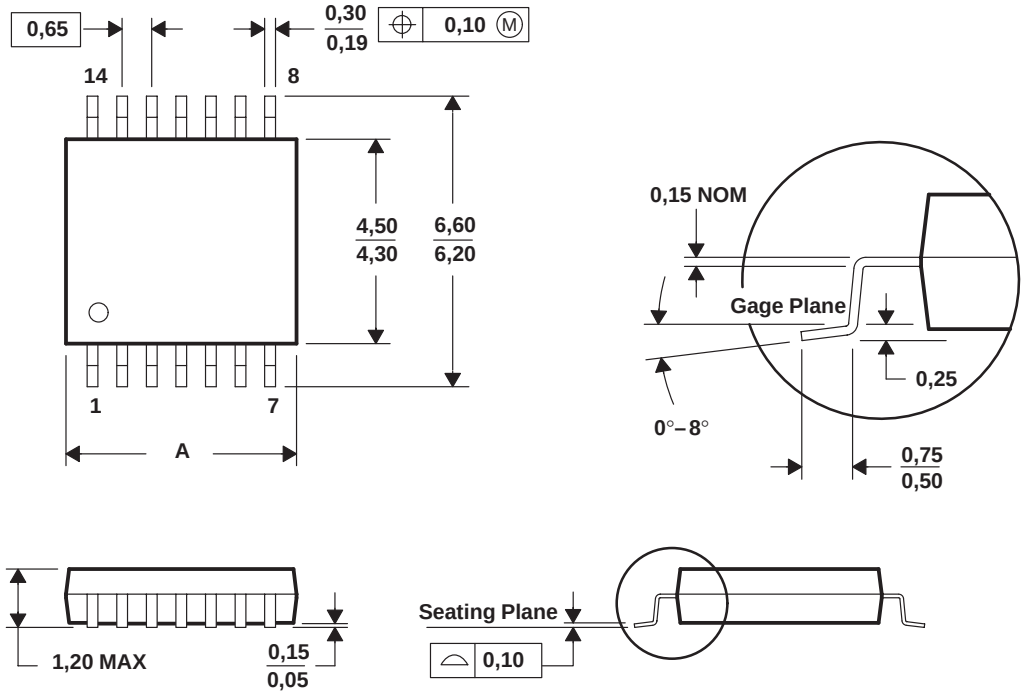


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HCT574QM96EP	SOIC	DW	20	2000	346.0	346.0	41.0
CD74HCT574QPWREP	TSSOP	PW	20	2000	346.0	346.0	33.0

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

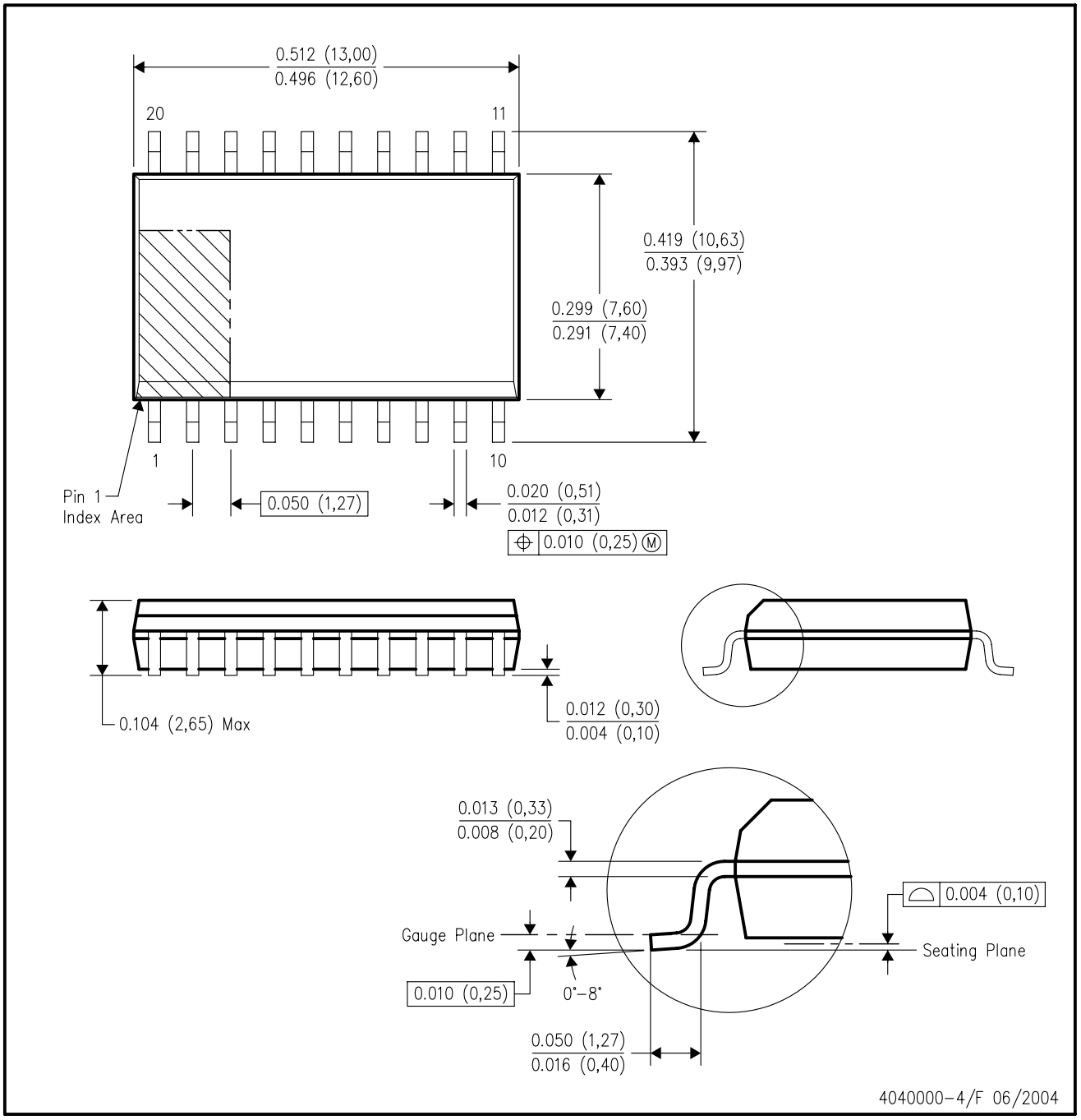


DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

DW (R–PDSO–G20) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

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